DESIGN AND IMPLEMENTATION OF LOW COST OPTICAL TRANSMITTER

A Thesis Submitted

in Partial Fulfillment of the Requirements

for the Degree of

DIIT

by

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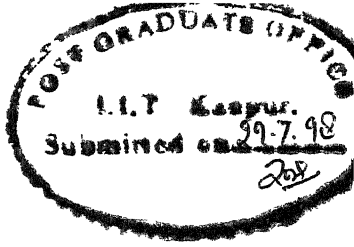

This is to certify that the thesis work entitled *'Design and Implementation of Low Cost Optical Transmitter'* by Pravas Ranjan Sahu(9712404) has been carried out under my supervision and the same has not been submitted elsewhere for a degree .

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(P.R.Sahu)

Abstract

Optical communication technology is growing rapidly with every passing day. It has several advantages over the conventional communication systems, which is drawing mass attention and an attempt is already underway to replace the existing systems by optical systems.

Here, an attempt is made to look into the design aspects of an optical transmitter for digital data transmission. The data is to be coded properly to ensure errorless detection at the receiver. For simplicity, manchester line coding scheme has been choosen. This project is mainly aimed to explore the basics involved in the design and implementation of a simple optical communication system.

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Chapter 1

Introduction

Possibilities of using optical signal for communication was suggested in late sixties [1]. Optical signals can be transmitted through atmospheric channel or through optical fibres. Optical fibres are made of glass and acts as waveguide for optical signals. The fibres used in optical communication have very large capacity (15 THz) [14] which can be utilised for carrying voice, data and video signal over long distances. The fibre-optic communication has many advantages over conventional copper based systems such as low crosstalk, high immunity to electromagnetic interference (EMI), high channel capacity, easy upgradability, security of the signal etc.. The loss in a fibre is much less compared to other conventional communication channels which makes optical fibre communication very much suitable for long distance communication link. This also minimises the requirement of number of repeaters and so is economic.

The fibre-optic communication is becoming attractive due to above mentioned advantages. Optical fiber is increasingly used not only for high speed communication links but also for transferring digital TV signal in TV studios, studio transmitter link (STL) and for

many other basic communication links. The cost of fibre-optic cables are becoming cheaper with passage of time. Therefore, optical communication is all set to play leading role in future for distribution of digital TV, Video conferencing and expansion of high speed data network.

1.1 Basic Lightwave Communication System

Three principal parts of a optical fibre communication system are the transmitter, the fibre and the receiver. The transmitter part consist of a light source with its associated driver circuitry which converts electrical data or signal information into a light signal preserving the same information contents. In intensity modulated (IM) system this is achieved by modulating the intensity of a light source by the information signal in a proportional relationship. Generally, the light source is a forward biased semiconductor junction diode. It can be either a Light Emitting Diode (LED) or a semiconductor Laser diode (LD). In both the cases the output light intensity holds a linear relationship with diode current, making intensity modulation possible. The LED works on the principle of recombination of holes and electrons in the conduction band with a controlled doping parameter. The energy that is librated during recombination appears in the form of radiation. The wavelength of this radiation lies in infrared region as communication links are generally operated with 850nm, 1350nm, 1530nm wavelengths. The Laser diode has two sharp facets which acts as mirrors. The active region lies in between the facets. When the device is operated, the mirrors provide feedback and the diode starts lasing. The emitted light is concentrated near the junction region, which makes possible the coupling of semiconductor light source into the fibre with reasonable efficiency.

The fibre carries the optical information from transmitter to receiver. Fibres are made

using very high quality glass. The lightwave travels through the fibre following the principle of total internal reflection and reaches at the other end with a little attenuation. The attenuation caused by a fiber is very less and can be as small as 0.2 dB/km [7].

The basic device used in a receiver to receive optical signal is a photo dectector. The photo detector is generally a reverse biased semiconductor junction diode. The lightwave incident on it can deliver energy to electron in the semicondutor crystal, exciting some of them into conduction band. The high electric field of the reverse biased junction region causes a current flow in the external circuit. The output current is proportional to the incident optical intensity and so replica of the modulating signal at the transmitter is available at the output of receiver.

The basic block diagram for an optical communication link is shown in Fig 1.1. The degradation of the signal due to fibre channel can be restored by the amplifier and signal conditioning section of the block diagram following the photodetector block.

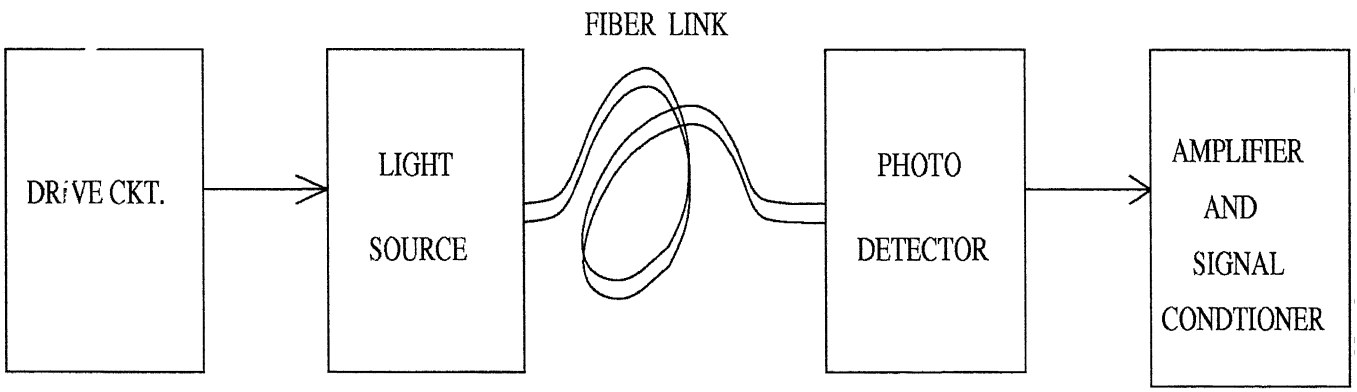


Figure 1.1: Basic System Block Diagram

1.2 Aim Of The Project

The project work deals with the data transfer between two PCs through optical fibre link. This work concentrates with the transmitter part of the system.

The entire block diagram of the system is shown in Fig. 1.2. The data is received from the serial port of computer terminal via a RS 232C connector. The data is to be received by a transmitter module and then transmitted to receive module after framing. After framing, data is coded suitably to ensure easy clock recovery at the receiver for synchronisation. Then, the coded data is transmitted by an optical transmitter. The transmitter converts data into a light signal and couples it to the fibre. The fibre carries the signal to the receiver at other end. The receiver receives the signal, does necessary wave shaping and then detects the data. Using the framing information, the data to be communicated to PC is retrived, which is then transferred to the computer terminal through RS 232C interface.

This project work assumes that the data is already available from the computer terminal. Also it is assumed that the cyclic redundancy check (CRC) check is done by the computer software to take care of any communication errors. The data received from computer is to be framed i.e., starting of frame and end of frame indication is to be inserted. Bit stuffing mechanism is needed to be incorporated to avoid confusion between data and starting/ending sequence. The line encoder block encodes data into a Manchester line code format. The manchester encoded signal is then transmited by the optical transmitter to the reciver. Design of transmitter and reciver are the major part of this work. The clock is to be recovered at the reciver for synchronisation and data decoding. The stuffed bits are also to be removed. The data is then to be transferred to the other computer.

The whole project work can be divided into the following steps.

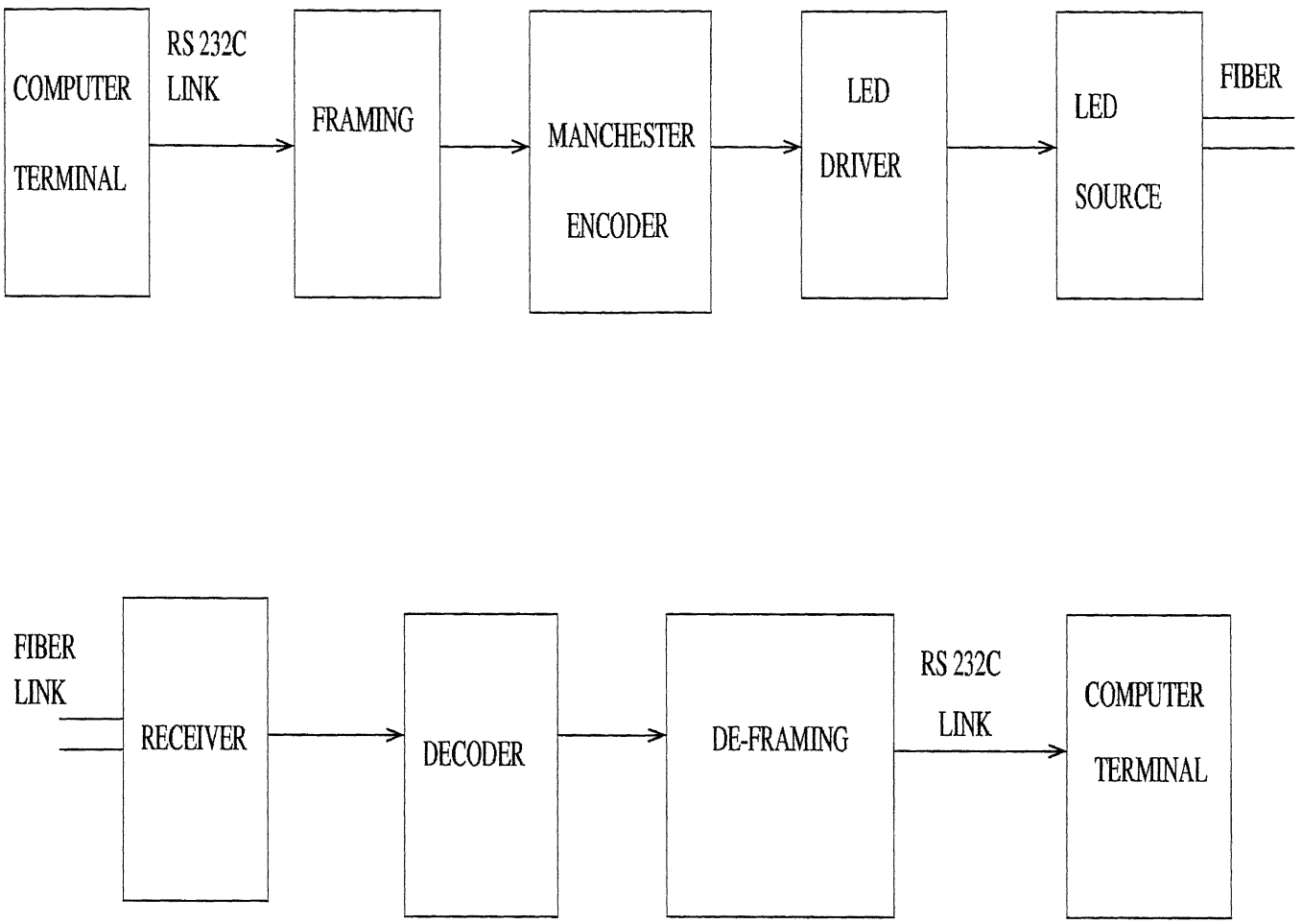


Figure 1.2: Complete System Block Diagram

1. Generation of starting and ending flag sequence.

2. Implementation of bit stuffing mechanism.

3. The manchester encoder implementation.

4. Design of optical transmitter.

Chapter 2

System Design

2.1 The Line Coding

2.1.1 Why Line Coding is required ?

A digital signal is subjected to dispersion, delay and attenuation, when it passes through a channel. Dispersion, delay and attenuation also increase with the increase in length of the channel. This is primarily due to limited bandwidth of the channel. The dispersion and delay offered by the channel results in intersymbol interference (ISI). When the signal is received by the receiver, the detector circuit samples the received signal at an instant when the ISI is minimum so as to make a decision either in favour of bit '1' or bit '0'. Hence, the receiver should have timing information. This information should be available with the received signal i.e, it should be possible to extract clock information from the received signal. For this reason, data bits are suitably coded at the transmitter before transmission. The type of codings used here are known as ' Line Coding '. Following are the desirable properties

of a line code [2]:

1. The signal after coding should have small transmission bandwidth.
2. For a given bandwidth and transmitted power, the code should be immune to channel noise and inter symbol interference (ISI).
3. It should carry information to detect and correct error in received data.
4. The power spectral density (PSD) of the transmitted signal should ideally match with the channel frequency response.
5. It should contain timing information which can be extracted at the receiver for transmitter and receiver synchronisation.

2.1.2 Various types of Line Codes

There are different types of line codes.They are as follows [2]:

1. In 'Polar' line coding a bit '1' is transmitted by a pulse $p(t)$, and a bit '0' is transmitted by a negative pulse $-p(t)$.
2. In 'ON/OFF' scheme a bit '1' is transmitted by a pulse $p(t)$ and a bit '0' is transmitted by no pulse.
3. In 'Bipolar', scheme a bit '1' is transmitted by a positive or negative pulse, depending on whether the previous '1' was transmitted by $p(t)$ or $-p(t)$. The rule is, if the previous '1' was transmitted by a pulse $+p(t)$, then the next '1' bit will be transmitted by a pulse $-p(t)$ and *vice versa*. The '0' bit is transmitted by no pulse.

4. In 'Duobinary' signalling a bit '1' is transmitted by a positive or negative pulse depending on the polarity of the previous pulse that was sent for bit '1' and the number of zeros between them. If the number of zeros between two successive '1s' is even, the present '1' bit will be encoded by the same pulse which was transmitted for previous '1' bit. If the number of zeros between two successive '1s' is odd, the present '1' bit will be encoded by the negative of the pulse which was transmitted for previous '1' bit. Bit '0' is transmitted by no pulse.

5. In Manchester line code, a positive pulse followed by a negative pulse of equal duration and amplitude is transmitted for a bit '1' and a negative pulse followed by a positive pulse for bit '0'. The width of each positive and negative pulse is half of the clock duration. This is shown in fig 2.1.

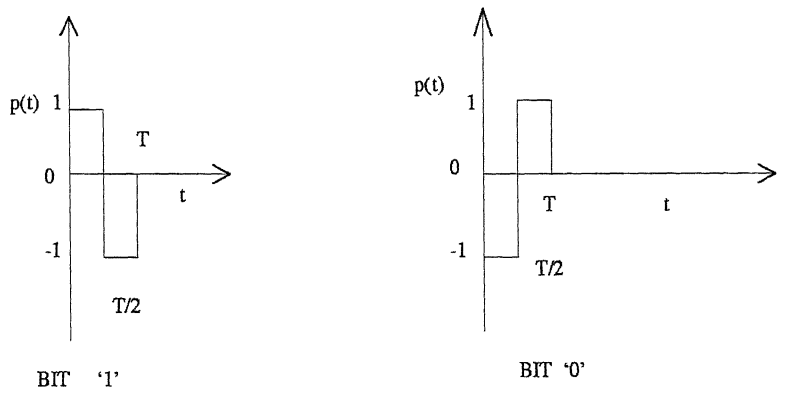


Figure 2.1: Manchester Coded Pulse

2.1.3 Manchester Coding implementation

The main motivation behind choosing manchester code is that its power spectral density (PSD) contains line component at clock frequency which can be used to recover the clock very easily using a Phase Locked Loop (PLL) circuit at the receiver. The block diagram of

the encoder unit is shown in fig 2.2. It consists of a two input EX-OR gate and a frequency doubler. The inputs to the EX-OR chip are the data input and a clock at twice the frequency of the system clock. The output of the EX-OR gate is the data output in the manchester encoded format.

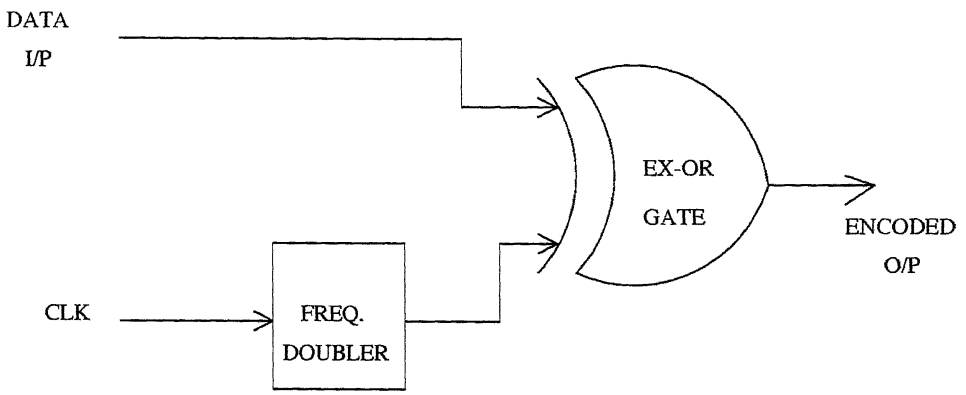


Figure 2.2: Block Diagram of the Manchester Encoder

2.1.3.1 Clock Frequency Doubler

The frequency doubler circuit is shown in fig 2.3. The circuit uses two operational amplifiers (TL 081)and an OR gate. The working of the circuit can be understood from the fig 2.4. The input clock pulse is integrated by the RC network. So, a triangular waveform appears at the input of the op-amps for each cycle of clock. The threshold voltages for op-amps are set using the variable potentiometers at V1 and V2 respectively, such that each op-amp output is a pulse at clock frequency with a phase shift. When V1 and V2 are properly set and the op-amp outputs are OR-ed, a clock signal at twice the input clock frequency can be obtained at the output of OR gate. Ideally, the circuit should act as a clock frequency doubler at 50 percent duty cycle. As the op-Amps are not identical, it will be difficult to have 50 percent

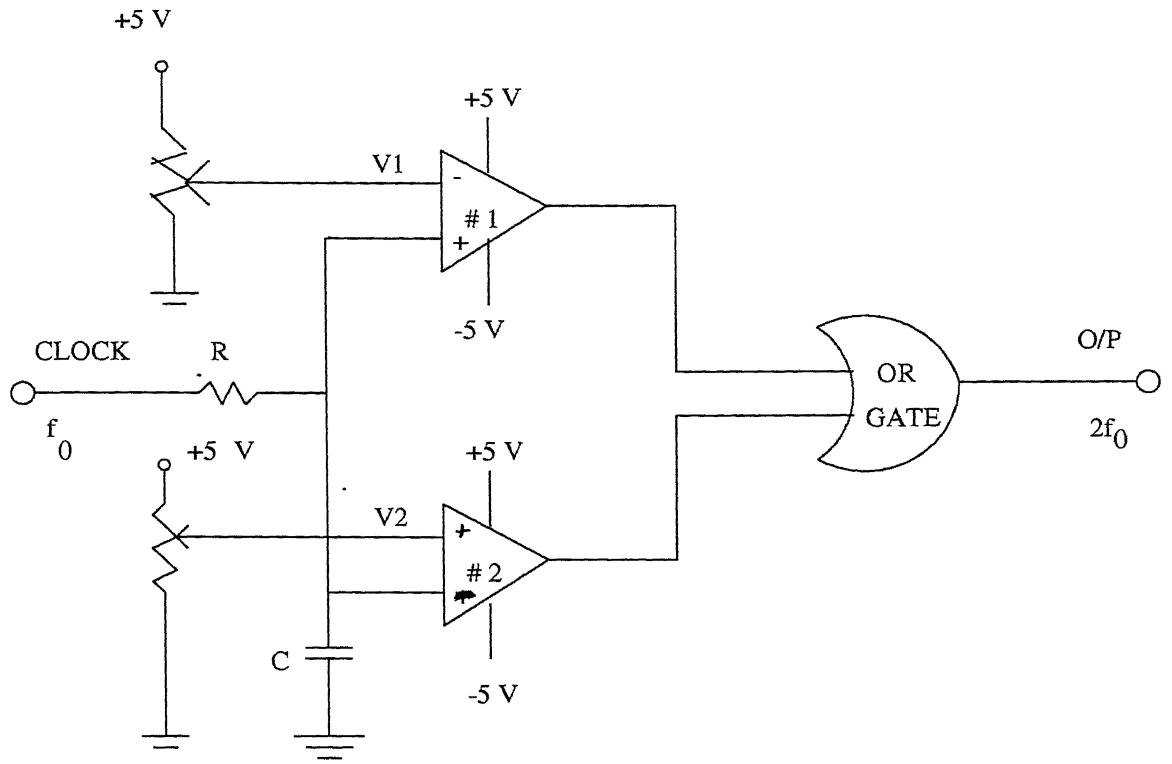


Figure 2.3: Frequency Doubler Circuit Diagram

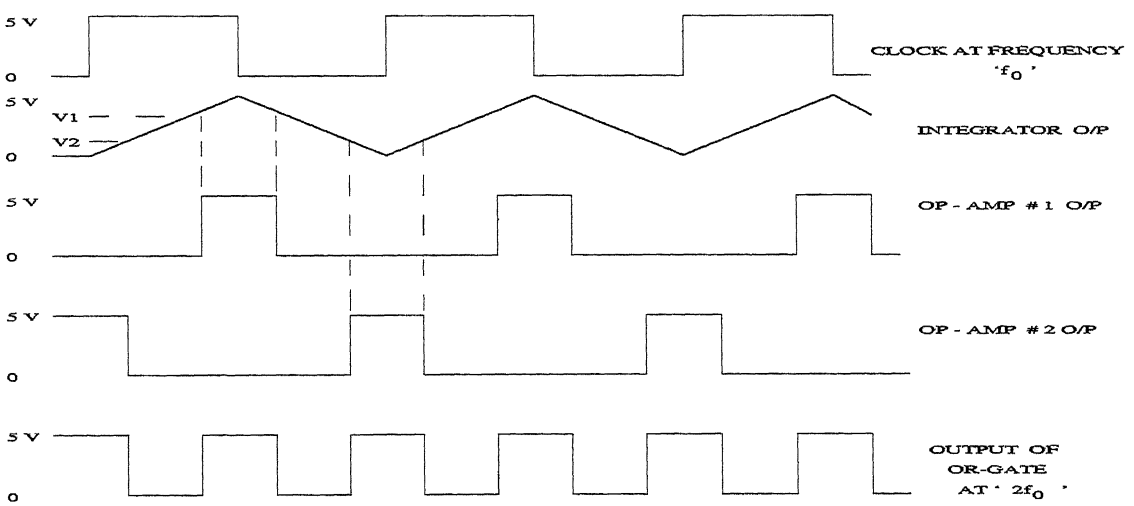


Figure 2.4: Frequency Doubler Circuit Waveform

duty cycle for output signal. Therefore, a monostable multivibrator (74S123) has been used to adjust the duty cycle exactly at 50 percent.

2.2 The Transmitter

Basically, there are two types of transmitters based on the input signal type i.e analog or digital. The analog transmitter requires analog input and the digital transmitter requires a digital input. Since, we are interested in establishing a communication link between PCs we are interested in digital data. Hence, here we consider only digital transmitters.

A transmitter has two major sections i.e., a source section and a drive section.

2.2.1 Source

An LED has been used as the light source for the transmitter. The LED MFOE71 has the peak of output spectrum at the wavelength of 820nm. Other characteristics are mentioned in the appendix A.

The maximum optical power that the LED can deliver is 3.5mW. Since, binary data is to be modulated, it has been operated in a ON/OFF mode. This modulation is called intensity modulation. The driver circuit for this is described below.

2.2.2 LED Drive Circuit

There are a number of driving circuits for digital data transmission purpose. A few are discussed below.

1. *Low impedance emitter follower circuit:* [9] This circuit is shown in fig 2.5. When an input pulse is applied to a properly biased transistor, it starts conducting and LED becomes ON. Thus, an intensity modulation is achieved. Optimum working of the circuit may be achieved by adjusting the R and C values.

2. *Low impedance drive circuit with shunt configuration :* [9] This circuit is shown in fig. 2.6. This circuit operation is controlled by the switching transistor, which is connected with the LED in parallel. Normally, the transistor is OFF. When an input pulse is applied at the base of the transistor it becomes ON. So, the current through LED gets a low impedance path and passes through it. The switching ON/OFF of the circuit depends on the collector resistance R of the transistor and the junction capacitance of LED.

3. *Transconductance Drive Circuit:* [9] This drive circuit is given in fig 2.7. Here, the LED is connected in series with the collector resistance of the switching transistor. The circuit converts an input base voltage into collector current. The circuit is biased for class A operation mode with quiscent collector current about half the peak value. The ON/OFF of the switching transistor controlles the LED operation.

4. For digital data transmission the ideal drive circuit may be a logic integrated circuit driver. A block diagram of such a circuit is shown in fig 2.8.

The frequency response of all drive circuits using switching transistors is poor at high frequencies due to space charge accumulation. The transistor drivers are not suitable for digital data transmission. Hence, integrated circuit drivers are preferred.

The LED driver used here is a line driver chip(74LS140). This is a two set of TTL 4-input NAND gate each having a maximum driving capacity of 60mA. Using both the sections of NAND gates a theoretical driving capacity of 120mA may be achieved. The chip has been

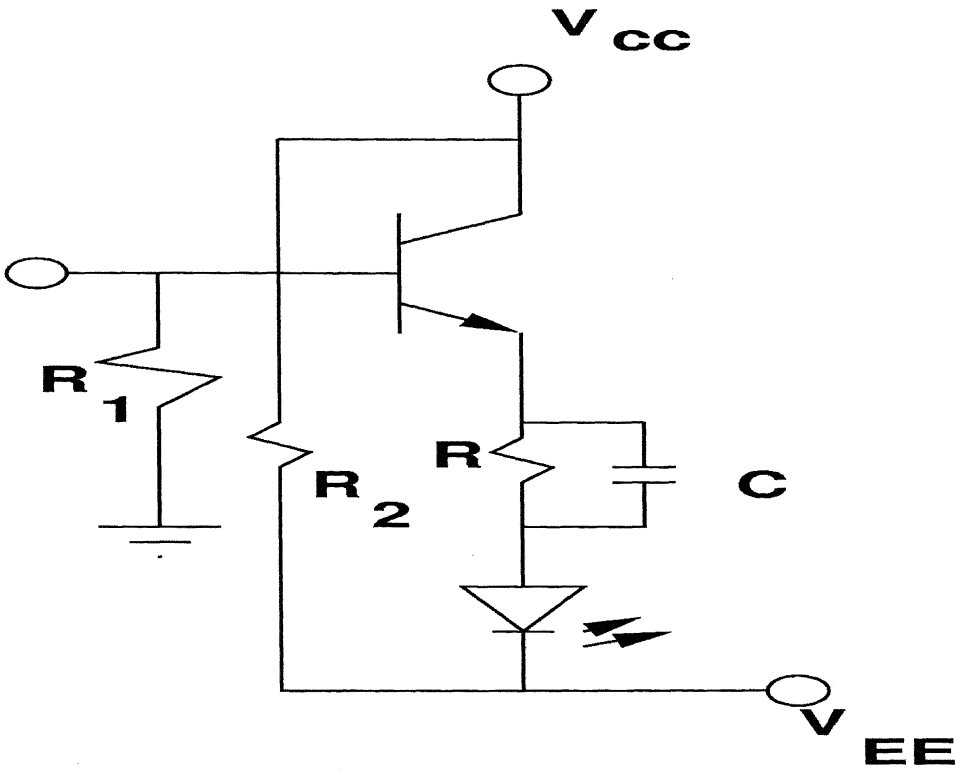


Figure 2.5: Low Impedance Emitter Follower Drive Circuit

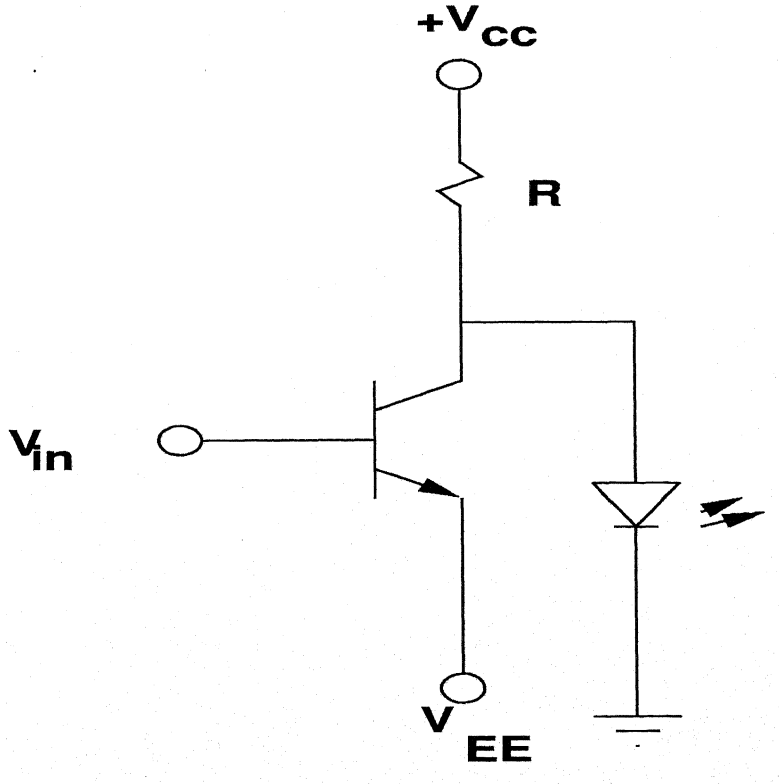


Figure 2.6: Low Impedance Shunt Drive Circuit

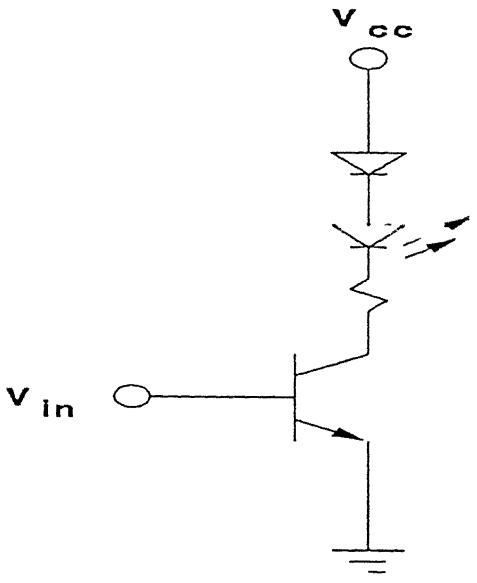


Figure 2.7: Common Emitter Transconductance Drive Circuit

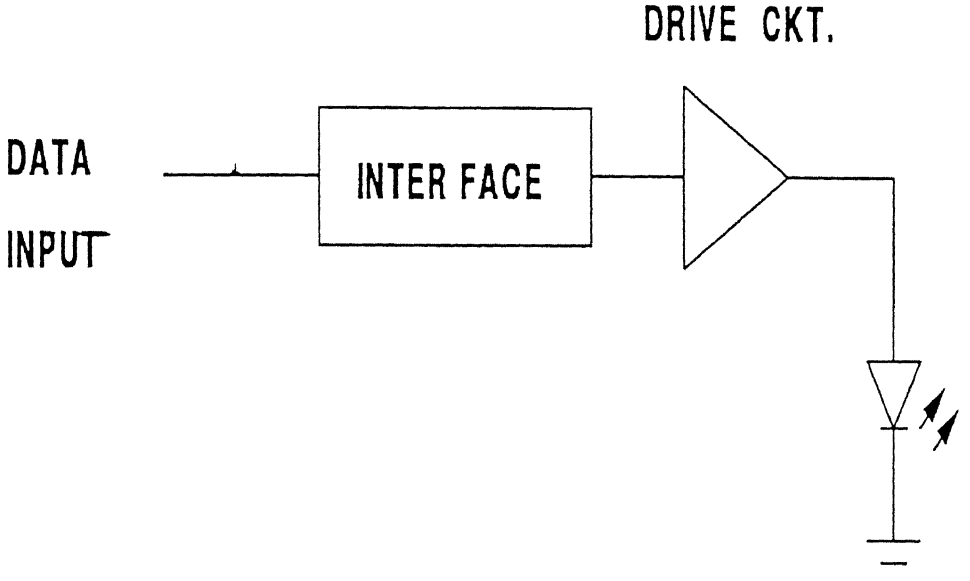
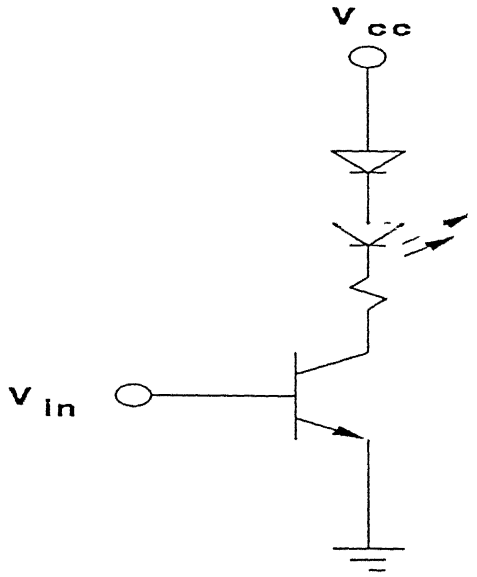


Figure 2.8: Logic Interfacing for Digital Transmission



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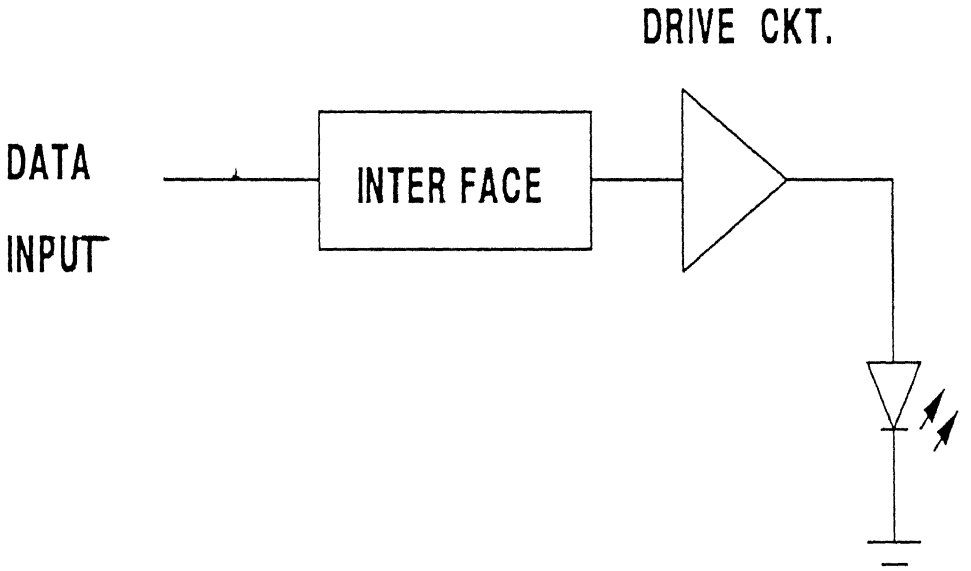

Figure 2.8: Logic Interfacing for Digital Transmission

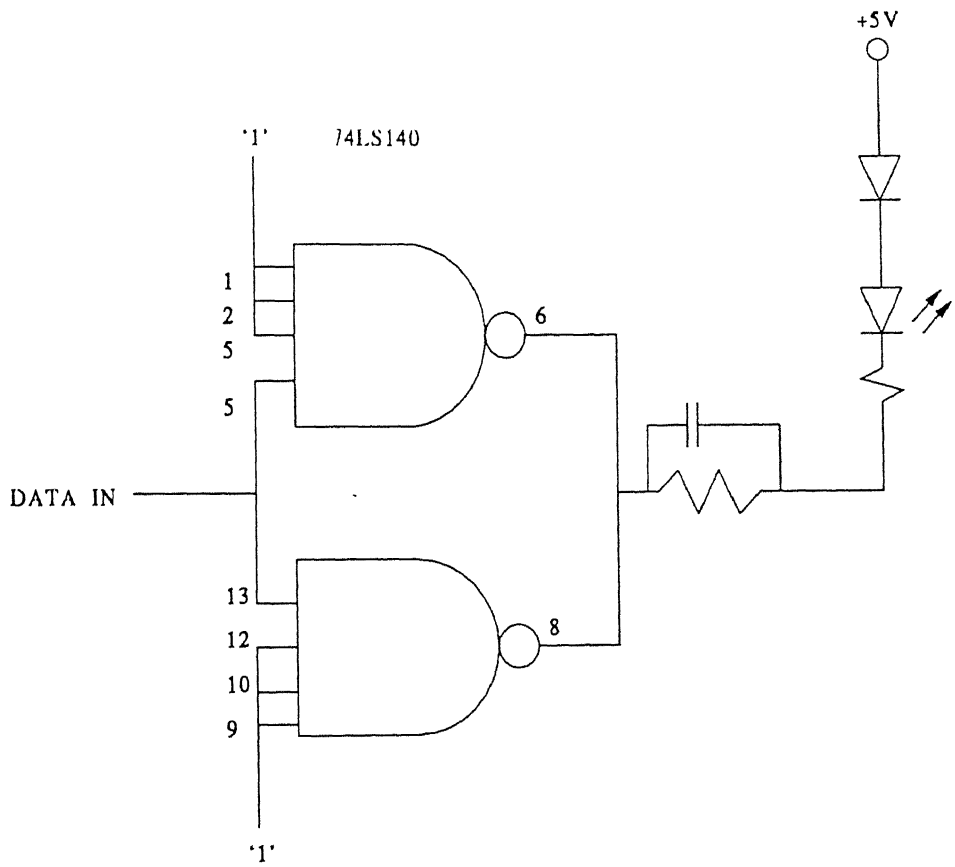

Figure 2.9: LED Drive Circuit

tested with a clock frequency from the function generator and gives satisfactory output upto 1.5 MHz. Consequently the link can be used upto bit rate of 750 KHz. The output of the driver circuit is applied to the LED source. This circuit is shown in fig. 2.9. LED switches ON/OFF depending on the presence or absence of the pulse output from the line driver and launches light information into the fibre. A capacitor is used at the output of the line driver for adequate wave shaping.

2.3 Fiber

The structure of an optical fiber is shown in fig 2.10. It is cyllindrical and flexible. It is made of two concentric layers of silica material having different refractive indices. The central layer is known as *core* and the outer layer is called *cladding*. The refractive index of core is higher than that of cladding. The refractive indices are so choosen that when a light ray enters into *core*, it gets reflected from the interface following the principle of 'total internal reflection' and propagates along the fiber. This mechanism is illustrated in figure 2.12.

The fibre is classified depending on the variation of the refractive index of the *core* and *cladding* material. If the refractive indices of the core and cladding are different but constant throughout their radial thicknessi, then the fiber is called step index (SI) fiber. If the refractive indices are a function of the radial thickness, then the fiber is called graded index (GI) fiber. The refracrive index profile for the SI and GI fibres are given in fig 2.11. Optical fibres can support a number of guided intensity profile called *modes*. A *single mode* fiber can guide only one intensity profile. *Multimode* fibres support more than one profile. *Single mode* fibres are important for applications where very high channel BW is required.

The total number of modes that an optical fiber can carry depends on the 'V' number [1],

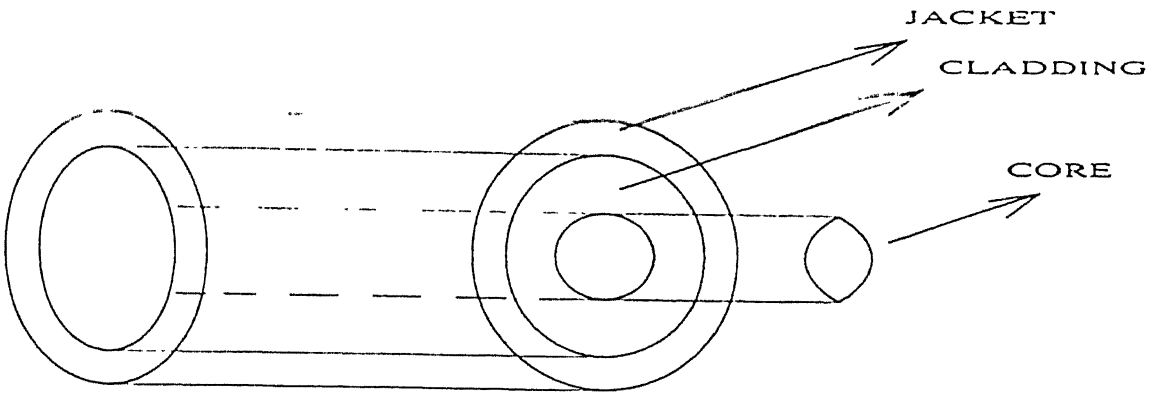

Figure 2.10: Fiber Structure

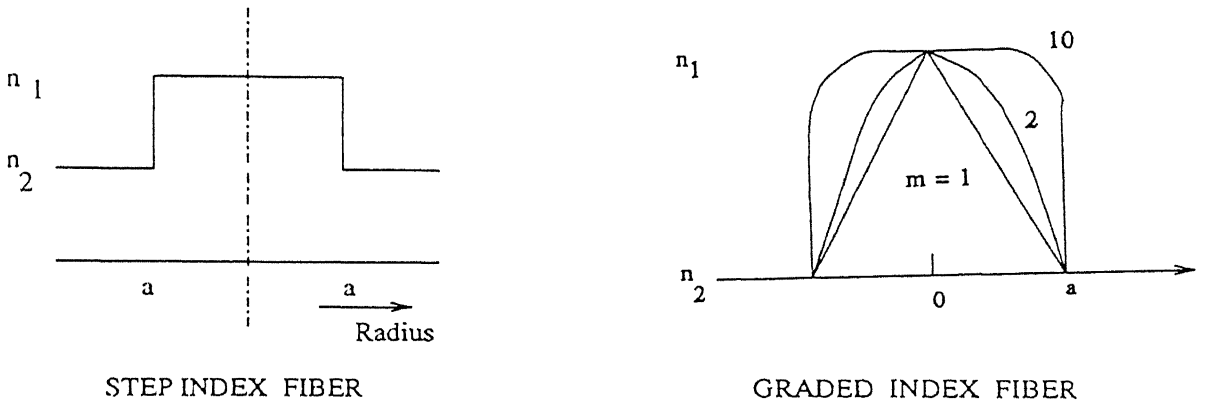

Figure 2.11: Refractive Index Profile of Fibers

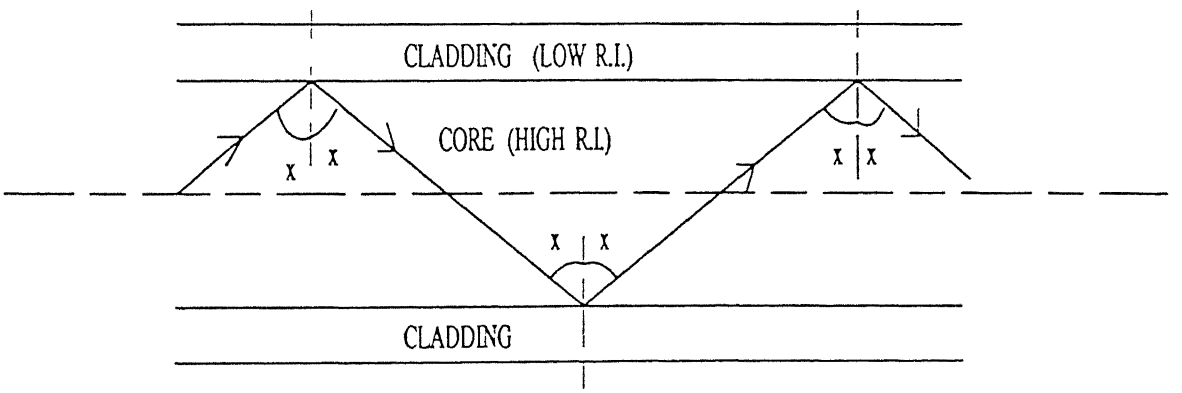

Figure 2.12: Total Internal Reflection of Light in Fiber

which is defined as

$$V = n_1 k a \sqrt{2(\Delta)}$$

Where, k= propagation constant

a=core radius

n_1=refractive index of core

Δ=measure of the relative difference between the maximum refractive index and its cladding value (n_2).

$$\Delta = \frac{(n_1)^2 - (n_2)^2}{2(n_1)^2}$$

2.4 The Receiver

A receiver is avaible for the detection and decoding purpose. A schematic block diagram is given in fig 2.13. A PIN photodetector diode(MFOD 71) has been used for detection purpose at the receiver. The specifications for the detector diode has been mentioned in appendix C. The detector produces an output current proportional to the light intensity coupled to it from the fibre. The detector is followed by a pre-amplifier which amplifies the weak signal produced by the detector. This is followed by a post amplifier which increases the signal strength to be used in subsequent stages. The next block derives the timing information from the received signal and is used for synchornisation and decoding of received signal in following stages. The decoder used here is a manchester decoder, which takes recovered clock and received data as inputs and decodes the same.

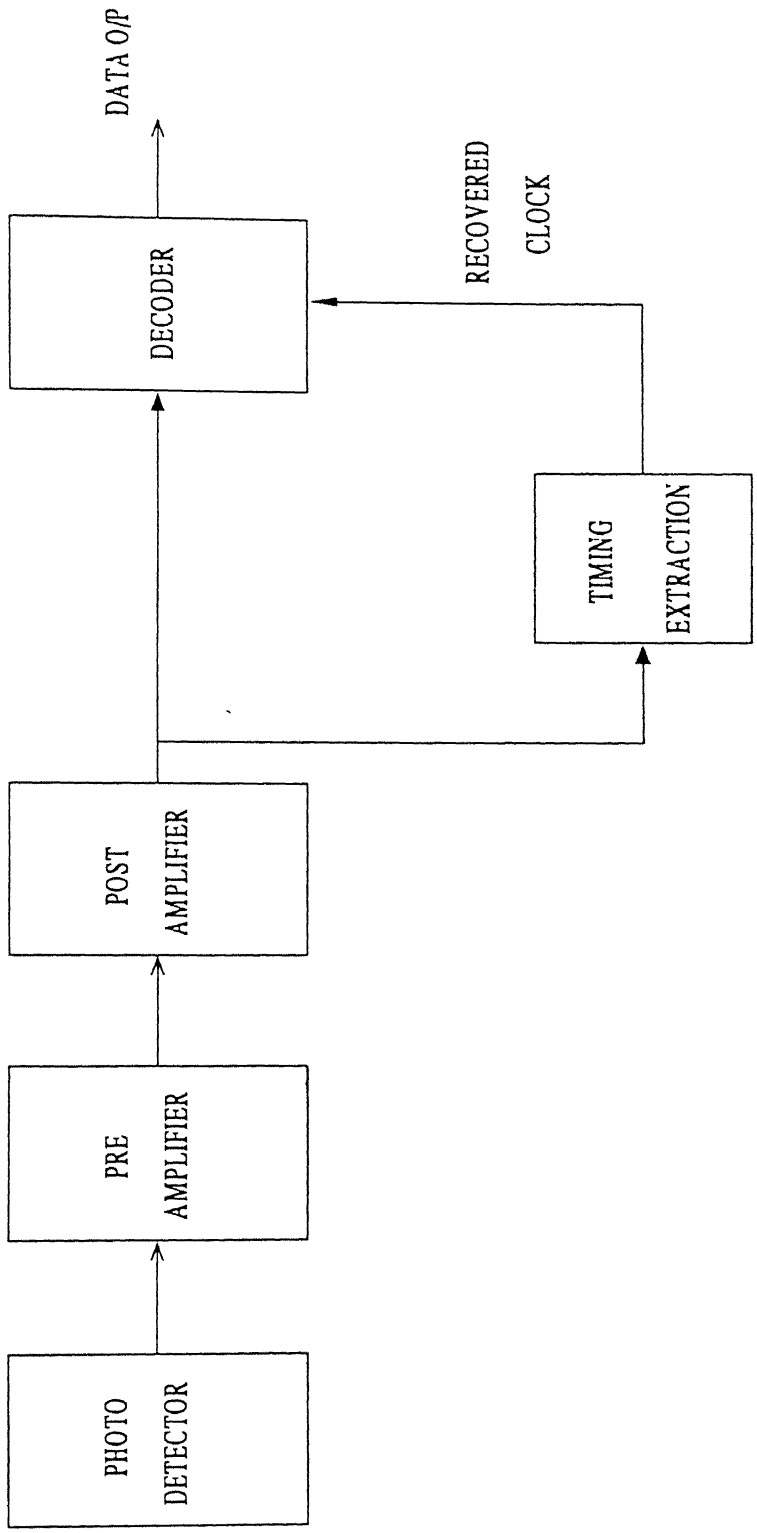

Figure 2.13: Schematic Block Diagram of Receiver

2.5 Framing

In data communication, there are two methods of data transfer. They are *Message switching* and *Packet switching* respectively. In *message switching*, the message is directly routed to its destination over the network passing through different nodes without any modification. At each node the message is received, stored and then forwarded to the next node when the link is available. *Message switching* has a number of demerits which gives rise to the need of packetization as follows: [8]

1. A message may be very long or very short. To accommodate the long message, large buffers need to be available. The hardware of these buffers is underused when short messages are received.

2. Even if a line is available, a switching computer will not begin to relay a message until the entire message has been received first i.e if the message duration is T and if required to be relayed R times then the minimum possible delay will be RT. Actual delay will be larger than this because the message has to wait in queue before being transmitted. For long messages and many relays it results in larger delays which is not desirable.

3. It may be possible that a link between two points is needed very briefly to accommodate a very short message but the link is already busy sending a long message. It would be useful to interrupt the long message for a short duration to allow the transmission of the short message. But this is not possible in message-switched system.

The above mentioned shortcomings of a *message switching* system can be avoided by a packet-switched network. In this method a message is divided into packets of fixed sizes. These packets are then transmitted.

2.5.1 What is Packetization ?

As stated above in *packet switching*, a long message is broken into many packets of equal length each, and then the packets are transmitted one after the other. Each transmitted packet is also added with some extra bits known as *overhead* meant for some special purpose. These additional bits carries information regarding its destination to enable the receiver to route it correctly. It also contains its source address so that the acknowledgement can be send back to the source. If a number of routes are available for packet switching then different packets may or may not take different routes to reach same destination depending on routing protocol. Thus in general packets may reach or may not reach at the destination in same orders. So, *overhead* should carry the sequence numbering information for easy reassembly.

2.5.2 Framing

In this project work it has been assumed that the message is received in packet format from the computer. The received packets are to be sent to the other computer terminal by our transmitter. Here the provision has to be made for the following points:

1. Preamble for sending timing information for synchronisation.

2. A starting of the frame (STX) sequence to be sent to the receiver. The receiver should identify the start of frame using this sequence. The sequence of binary digits used for STX should not be there any where in the data (see fig 2.14).

3. An end of frame (ETX) sequence to be sent to the receiver to mark the end of frame. This is also a specific sequence of binary bits and should not repeat in the data.

4. It is possible to represent both STX and ETX flag by same bit sequence. In order to

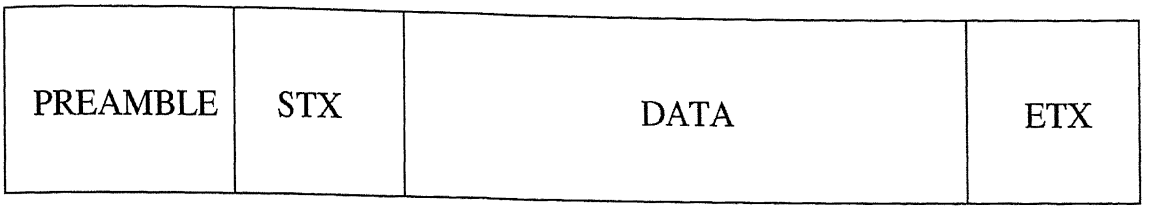

Figure 2.14: Frame Structure

avoid this bit sequence in data, bit stuffing can be used.

2.5.3 Bit Stuffing Mechanism

Bit stuffing is a method adopted in data transmission to avoid confusion between data sequence in a frame and starting and ending flag sequences. For example, if the STX flag is decided to be a sequence of a '0' followed by a sequence of five '1s', then care must be taken that the same sequence should not appear within a frame of the data sequence. So, a check must be carried out to see if the same sequence is there in a data sequence and when it appears it should be modified to avoid confusion.

2.5.4 Bit Stuffing Procedure

As stated above to prevent the STX (ETX) sequence to appear in the data sequence, modification is to be made in data wnen the STX (ETX) sequence occurs in it. This is achieved by incorporating a checking mechanism that compares the data sequence with the flag sequence and adds a '0' bit just before the last bit of each data sequence which matches with the flag sequence. Thus if we consider our flag sequence to be a '0' followed by a sequence of five consecutive '1s' then our logic circuit should keep on counting the number of 1s in a data stream and when atleast four ones appear in a succession it should add a '0' before

the fourth '1'. The same check can also be done to prevent end of frame (ETX) sequence to appear in the data stream in a frame.

2.6 Circuit Assembly and Testing

The transmitter has been implemented in various stages.

1. The clock frequency doubler circuit assembled using op-amps, OR-gate and a monostable multivibrator as described in section 2.1 and fig 2.3. The input clock frequency is 150KHz. Therefore, the output was exactly 300KHz. The monostable multivibrator is used to adjust the pulse width for 50 percent duty cycle.

2. The Manchester encoder circuit is implemented using the frequency doubler and an EX-OR gate as described in section 2.1 and fig 2.1.

3. The LED driver circuit is assembled as described in section 2.2 and circuit diagram in fig 2.9. It is tested with the input from a function generator and the output was observed with an oscilloscope. Later, the manchester encoded data was fed and the transmitted sequence was observed at the receive end.

4. The LED source is connected with the driver as shown in the diagram in fig 2.9.

2.6.1 PRBS Generator for testing :

A pseudorandom bit sequence (PRBS) generator is implemented using three bits of a 4-bit shift register (74LS194) and a clock frequency of 150 KHz as shown in fig 2.15. It generates

a sequence 0,0,1,0,1,1,1..(repeats). This sequence is used as input for transmitter.

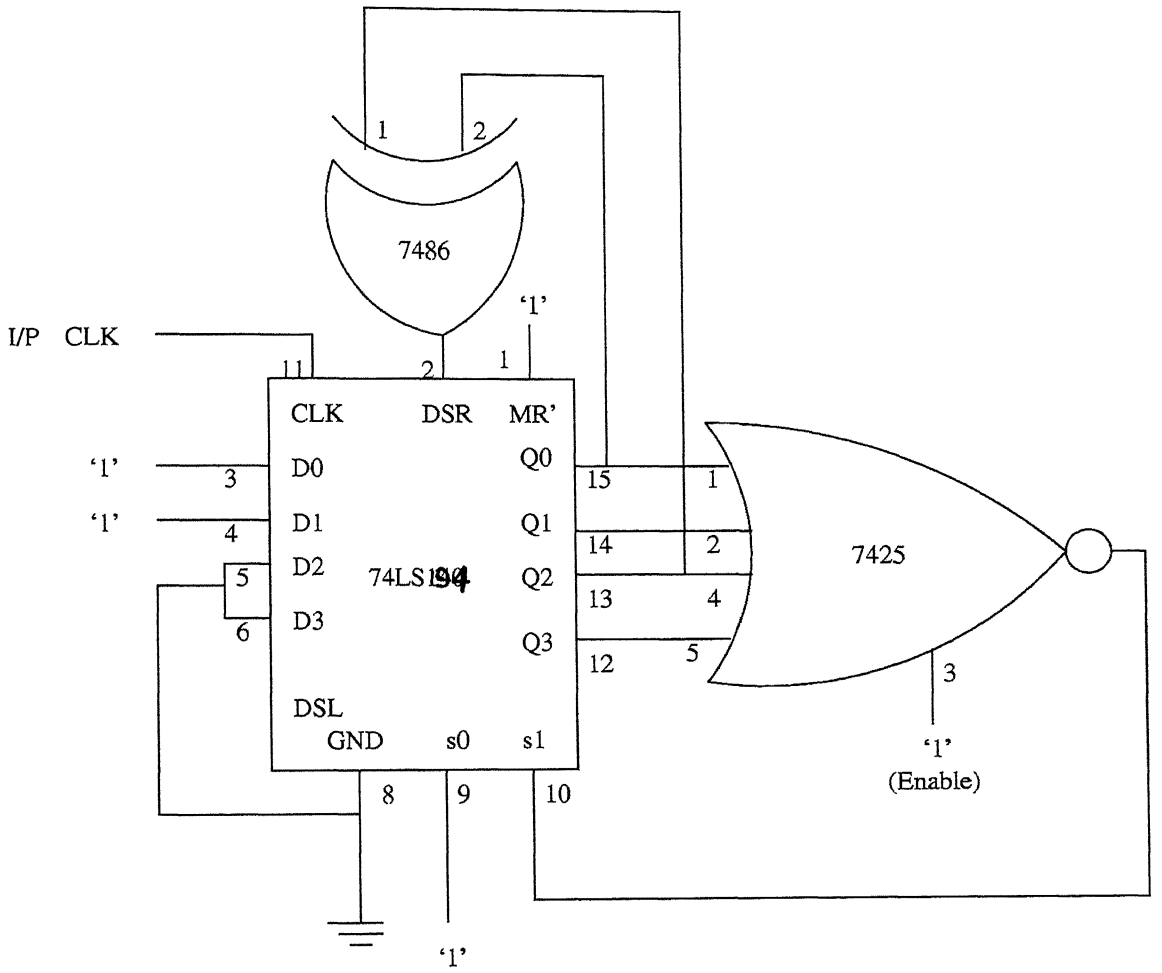

Figure 2.15: PRBS Circuit Diagram

Chapter 3

Performance of the transmitter

1. The pseurandom bit sequence(PRBS) generator performs satisfactorily. Presently, the number of bits of the sequence are seven only. The sequence bits can be increased to '15' if we use the fourth bit of the shift register. This has been tested practically and the sequence has been found to be 1,1,1,1,0,1,0,1,1,0,0,1,0,0,0....(repeats). Addition of more shift registers will increase the number of bits exponentially $(2^n - 1)$.

2. The clock frequency doubler circuit performs well individually. The duty cycle is very close to 50 percent. But since the op-amp inputs are adjusted assuming the integrator output a *triangle wave*, which is not true practically (as there will always be a difference between the charging and discharging envelopes of the capacitor), a good quality integrator may be used to improve the stability and duty cycle of the doubler. However, the monostable multivibrator with adjustable pulse width is capable of maintaining the duty cycle at 50 percent. Another demerit of this circuit is that this can double only a particular frequency for which it has been designed. Any drift in input clock frequency gets reflected in the output. Thus a stable input clock may

give a better result.

3. The Manchester encoder output gives the coded output of the PRBS sequence. As long as the clock frequency of the frequency doubler remains stable the encoded output remains stable.

4. The drive circuit using a line driver gives excellent result upto a frequency of 1.5MHz with a clock from the function generator. The function generator output shape distorts beyond this frequency which distorts the line driver output. A stable input clock may also give good response above this frequency. Therefore, the link can be used upto a bitrate of 750 kbps. But a manchester encoder is needed to be designed for 750 kbps.

Chapter 4

Conclusion and Discussion

The transmitter has been designed and tested for a data rate of 300 kbps. The source rise time response is 25 ns. Thus, it can individually transmit data at a rate of 14 Mbps. The maximum receiver response time is 5 ns. So, it can also individually receive data at a rate much above the maximum transmission rate of the source. The length of the fiber being 1 m, the dispersion and other attenuation can be neglected. Hence, the limitation on the bit rate may be due to the poor response time of the transmitter drive circuitry. It has been confirmed practically that the line driver response is very poor above 1.5 MHz. Another reason may be due to the instability of the function generator output above 1.5 MHz. If a stable function generator is used, then a higher bit rate may be achieved. The clock frequency doubler also limits the bit rate of the system. A stable integrator may be used in place of the simple RC network of the frequency doubler circuit to improve the bit rate.

Implementation of the 'framing' by generating STX and ETX sequences is a future possible extension of work.

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Appendix A

LED Specification

The transmitter source used here is an infrared LED of wavelength 820nm. Following are the specifications from the manufacturer's data sheet.

- LED - MFOE 71
- Power output - 3.5 mW.
- Rise and fall time - 25 ns.
- Wavelength - 820nm.
- Reverse breakdown voltage - 4.0 Volts.
- Forward voltage - 2.0 Volts.
- Package - 2 pin PCB mountable package with fibre alignment and locking mechanism.
- Maximum Reverse voltage - 6.0 Volts.
- Forward current - 60 mA (continuous). 1A (peak pulse).
- Total power dissipation - 150 mW @ $T_a = 25^0$C, 2 mW/^{0}C (derate above 25^0C).

Appendix B

Fiber Specification

- Plastic fiber of 1mm diameter.
- Fiber profile - Step index.
- Core material - High purity polymethyle metacrylote (R.I.=1.491) [16].
- Cladding material - Special transparent fluorine polymer.
- Protection cover - Black poly-ethelyne jacket.
- Length - 1 m.

Appendix C

Detector Specification

A PIN photodiode is used here for detection purpose. This is designed for detection of infrared radiation in fibre optic system.Specifications obtained from manufacturer's data sheet are given below :

- PIN photodetector diode - MFOD 71.
- Responsivity - 0.2 uA / uW.
- Peak wavelength - 820 nm.
- Reverse breakdown voltage - 100 Volts.
- Dark current - 10 nA.
- Forward voltage - 1.1 V at forward current of 50 mA.
- Maximum response time - 5 ns.
- Total power dissipation - 150 mW @ $T_a = 25^0$C(derate above 25^0C).

Appendix D

System Design Consideration

D.1 Required Specifications

For the design of a fiber-optic system following specifications are required [14]:

1. Type of signal to be used.
2. Link length required.
3. Tolerable SNR, BER, rise/fall time .

D.2 Calculations

Based on the specifications following calculations are to be done :

1. Preliminary link power budget.
2. Preliminary rise/fall time budget.
3. Final link power budget.

4. Final rise/fall time budget.

Based on the above calculations finally, component specifications are choosen.

D.2.1 Link power budget calculation

Link power budget is calculated by investigating the attenuations of an optical signal due to the discontinuities from source to detector. Following are the points where attenuations are to be found out:

1. At source to fiber coupling.
2. Between the ends of a fixed length of fiber.
3. At the fiber to fiber joints.
   (a) At permanent joints.
   (b) At connectors.
4. At fiber to detector coupling.

The net power incident on the detector = Source power - Total attenuation.

A noise margin (usually 2.5 dB for 0 to 50^0C) is required to be included.

D.2.2 Rise/Fall time budget

Overall rise/fall time of the system $= 1.1\sqrt{(T_x)^2 + (T_f)^2 + (T_r)^2} = \frac{0.35}{BW}$

Where,

(T_x)= Transmitter rise time.

(T_f)= Fiber rise time.

(T_r)= Receiver rise time.

For design,

the maximum acceptable rise/fall time $T_m = 0.7T_r = \frac{0.025}{BW}$

Finally, component specification is to be determined. These specifications include all requirements associated with environmental, electrical power and signal, optical power and signal and bandwidth constraints. This also includes the requirements imposed by the link power budget and rise/fall time budget computations. Once the component specifications are done, the system can be assembled.

Appendix E

Complete Circuit Diagram of the Transmitter

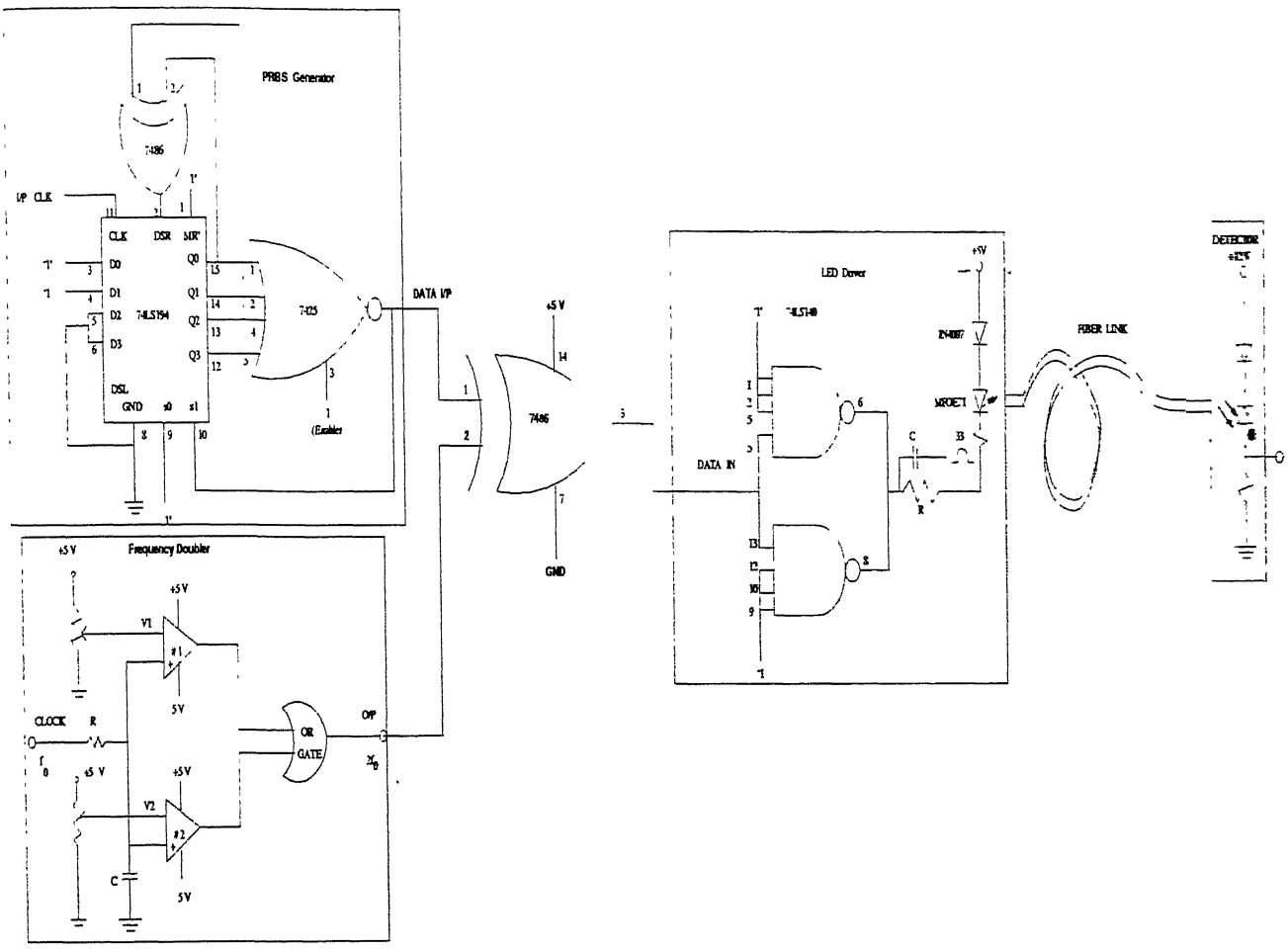

Figure E.1: Complete Circuit Diagram of the transmitter